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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,931	02/12/2002	Shunpei Yamazaki	740756-2433	3751

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,931	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-80* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims withdrawn from consideration are 1-9,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40,42,44,46,48,50,52,54,56,58,60,62,64,66,68,70,72,74 and 76.

Continuation of Disposition of Claims: Claims rejected are 10,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63,65,67,69,71,73,75 and 77-80.

DETAILED ACTION

This Office Action is in response to the amendment filed on 2/22/05. Currently, claims 1-80 are pending. Claims 10, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 75 and 77-80 are elected.

EXAMINER'S REMARKS

The Examiner would like to further clarify for the record that the elected claims, 47, 51, 53, 55, 59, and 63, and generic claim 78, are drawn to figures 2A-2G. In addition, claims 10, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 49, 57, 61, 65, 67, 69, 71, 73, 75 and 77, also read on figures 2A-2G, as a result, will be examined on the merits.

Election/Restrictions

Applicant's election without traverse of claims 47, 51, 53, 55, 59 and 63 (figures 2A-2G) in the reply filed on 3/24/03 is acknowledged.

Claims 1-9, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72, 74, 76, are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species (figures 1A-1G), there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 3/24/03.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 11/15/04 was filed after the mailing date of the Office Action on 4/23/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to show the second semiconductor film containing a noble (rare) gas element. In addition, the drawings fails to show, what appears to by two additional semiconductor films one having amorphous structure and another having a crystalline structure as described in the specification (See figures 2A-2G, page 17, lines 2-8). Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as

"amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 43, 75 and 77-80, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is indefinite whether "an upper layer" is an additional layer formed on the second semiconductor film, or if "an upper layer" is formed on an upper surface of the second semiconductor film.

Claim 43 recites the limitation "third semiconductor film" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 80 recites the limitation "...a noble gas element on the first semiconductor film." in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 11 13, 15, 17, 19, 21, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 53, 55, 57, 59, 61, 63, 65, 67, 71, 73, 75 and 77-80, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 5,789,284 in view of Chan US Patent 6,670,259.

Yamazaki discloses the semiconductor method substantially as claimed. See figures 1A-9C, and corresponding text, where Yamazaki shows, pertaining to claim 10, a method of manufacturing a semiconductor device comprising the steps of: adding a metallic element **104** to a first semiconductor film **103** having an amorphous structure (figure 1A; col., 6, lines 9-23); crystallizing the first semiconductor film to form a first semiconductor film having a crystalline structure **105** (figure 1B; col. 6, lines 24-34);

forming a barrier layer **106** on a surface of the first semiconductor film having a crystalline structure (figure 1C; col. 6, lines 43-58); forming a second semiconductor film **107** on the barrier layer (figure 1C; col. 6, lines 65-67); gettering the metallic element into the upper layer of the second semiconductor film to remove or reduce the amount of the metallic element within the first semiconductor film having a crystalline structure (figure1C-1D; col. 7, lines 10-15); and removing the second semiconductor film (figure 1D; col. 7, lines 56-67; col. 8, lines 1-10). In addition, Yamazaki shows, pertaining to claim 47, a method of manufacturing a semiconductor device comprising: forming a first semiconductor film **105** having an amorphous structure over a substrate **101** (figure 1A; col. 6, lines 9-23); providing the first semiconductor film with a material **104** for promoting crystallization (figure 1A; col. 2, lines 50-55; col. 6, lines 1-8, 20-23); heating the first semiconductor film for crystallizing (figure 1B; col. 6, lines 24-34); irradiating the first semiconductor film with a laser light for improving crystallinity (col. 12, lines 28-44); forming a barrier layer **106** over the first semiconductor film having a crystalline structure (figure 1C; col. 6, lines 43-57); forming a second semiconductor film **107** over the barrier layer (figure 1C; col. 8, lines 27-35); gettering the material for promoting crystallization into the upper layer of the second semiconductor film (figure1C-1D; col. 7, lines 10-15). Also, Yamazaki shows, pertaining to claim 49, a method of manufacturing a semiconductor device comprising: forming a first semiconductor film **103** having an amorphous structure over a substrate **101** (figure 1A; col., 6, lines 9-23); providing the first semiconductor film with a material **104** for promoting crystallization (figure 1A; col. 2, lines 50-55; col. 6, lines 1-8, 20-23); heating the first semiconductor film for crystallizing (figure 1B; col. 6, lines 24-34); irradiating the first semiconductor

with a laser light for improving crystallinity (col. 12, lines 28-44); forming a second semiconductor film over the first semiconductor film **107** (figure 1C; col. 8, lines 27-35); gettering the material for promoting crystallization into the second semiconductor film (figure1C-1D; col. 7, lines 10-15). Yamazaki shows, pertaining to claims 67 and 78, a method of manufacturing a semiconductor device comprising the steps of: providing a crystalline semiconductor film **105** comprising silicon over a substrate **101**, said crystalline semiconductor film containing a metallic element **104** (figure 1A; col., 6, lines 9-23) ; forming a barrier layer **106** over the crystalline semiconductor film (for claim 67, figure 1C; col. 6, lines 43-58); forming a semiconductor film **107** over the crystalline semiconductor film ; gettering the metallic element into the semiconductor film to remove or reduce the amount of the metallic element within the crystalline semiconductor film (figure1C-1D; col. 7, lines 10-15). Also, Yamazaki shows, pertaining to claim 13,wherein the second semiconductor film is a semiconductor film having an amorphous structure or a crystalline structure. Yamazaki shows, pertaining to claim 15, wherein the metallic element is one element or a plurality of elements chosen for the group consisting of Fe, Ni, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au. In addition, Yamazaki shows, pertaining to claim 17, wherein the step of crystallizing the first semiconductor film is a heat treatment process. Also, Yamazaki shows, pertaining to claim 19, wherein the step of crystallizing the first semiconductor film is a process of irradiating strong light to the semiconductor film having an amorphous structure. Yamazaki shows, pertaining to claim 21, wherein the step of crystallizing the first semiconductor film is a heat treatment process and a process of irradiating strong light to the semiconductor film having an amorphous structure. In addition, Yamazaki shows, pertaining to claims 25, 53 and 71,

wherein the step of forming a barrier layer is a step of oxidizing a surface of the (first, for claims 53 and 71) semiconductor film having a crystalline structure by irradiating ultraviolet light. Also, Yamazaki shows, pertaining to claim 27, wherein the step of gettering is a heat treatment process. Yamazaki shows, pertaining to claim 29, wherein the step of gettering is a process of irradiating strong light to the semiconductor film. In addition, Yamazaki shows, pertaining to claim 31, wherein the step of gettering is a heat treatment process and a process of irradiating strong light to the semiconductor film. Also, Yamazaki shows, pertaining to claims 33, 35, 37 and 39, wherein the strong light is emitted from a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. Yamazaki shows, pertaining to claim 43, wherein the third semiconductor film further comprises one element or a plurality of elements selected from the group O, O_2, P, H, H_2. Finally, Yamazaki shows, pertaining to claims 63, 65 and 77, wherein the semiconductor device is applied to an electronic apparatus selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a DVD, a digital camera, a front type projector, a rear type projector, a mobile phone, and an electronic book.

However, Yamazaki fails to show, pertaining to claims 10, 47, 49, 67, and 78-80, adding a noble gas element to an upper layer of the (second, for claims 10, 47 and 49) semiconductor film. In addition, Yamazaki fails to show, pertaining to claim 11, comprising the step of adding one element or a plurality of elements chosen from the group consisting of O, O_2, P, H and H_2 in addition to the noble gas element. Also, Yamazaki fails to show, pertaining to claims 41, 55, 57 and 73, wherein the noble gas

element is at least an element selected from the group consisting of He, Ne, Ar, Kr and Xe. Finally, Yamazaki fails to show, pertaining to claims 45, 59, 61 and 75, wherein the second semiconductor film comprises the noble gas element at a concentration of 1 x 10^{19} to 1x $10^{22}/cm^3$.

Chan teaches, in figures 1A-5, and corresponding text, that the inert atoms, such as helium, neon, argon, krypton and xenon, are implanted into the upper surface of the mono crystalline silicon film to form a damage layer. The damage layer is formed for the purpose of creating, defects, gaps or holes, resulting in gettering sites for the removal of impurities within a silicon film (col. 1, lines 34-41; col. 4, lines 58-65; col. 5, lines col. 6, lines 1-50; col. 7, lines 45-51; col. 8, lines 1-23).

It would have been obvious to one of ordinary skill in the art to incorporate the follow: (1 adding a noble gas element to an upper layer of the (second) semiconductor film; (2 wherein the noble gas element is at least an element selected from the group consisting of He, Ne, Ar, Kr and Xe; (3 comprising the step of adding one element or a plurality of elements chosen from the group consisting of O, O_2, P, H and H_2 in addition to the noble gas element; (4 wherein the second semiconductor film comprises the noble gas element at a concentration of 1 x 10^{19} to 1x $10^{22}/cm^3$, in the method of Yamazaki, pertaining to claims 10, 11, 41, 45, 47, 49, 55, 59, 61, 67 , 73, 75, and 78-80, according to the teachings of Chan, with the motivation of creating gettering sites as taught by Chan, for the purpose of removing impurities such as, copper, nickel, silver, from the first semiconductor film, thereby dramatically improving the crystallized semiconductor film for an active region within a semiconductor device.

Claims 23, 51 and 69, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 5,789,284 in view of Chan US Patent 6,670,259 in further view of Bhat et al., US Patent 6,291,888.

Yamazaki in view of Chan, discloses the semiconductor method substantially as claimed. See preceding rejection of claims 10, 13, 15, 17, 19, 21, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 53, 55, 57, 59, 61, 63, 65, 67, 71, 43, 75 and 77-80, under 35 U.S.C. 103(a).

However, Yamazaki in view of Chan, fail to show, pertaining to claims 23, 51 and 69, wherein the step of forming the barrier layer is a step of oxidizing a surface of the semiconductor film having a crystalline structure by using a solution containing ozone.

Bhat teaches, a thermal oxide film that may be formed by conventional techniques (col. 6, lines 12-15).

It would have been obvious to one of ordinary skill in the art to, incorporate, wherein the step of forming the barrier layer is a step of oxidizing a surface of the semiconductor film having a crystalline structure by using a solution containing ozone, in the method Yamazaki in view of Chan, pertaining to claims 23, 51 and 69, according to the teachings Bhat, with the motivation of creating an oxide film, whether the oxide film is formed by ozone or thermal oxidation, etc., would prove to be equivalent since the ultimate result would be to create an oxide film as a barrier layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
May 10, 2005

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812